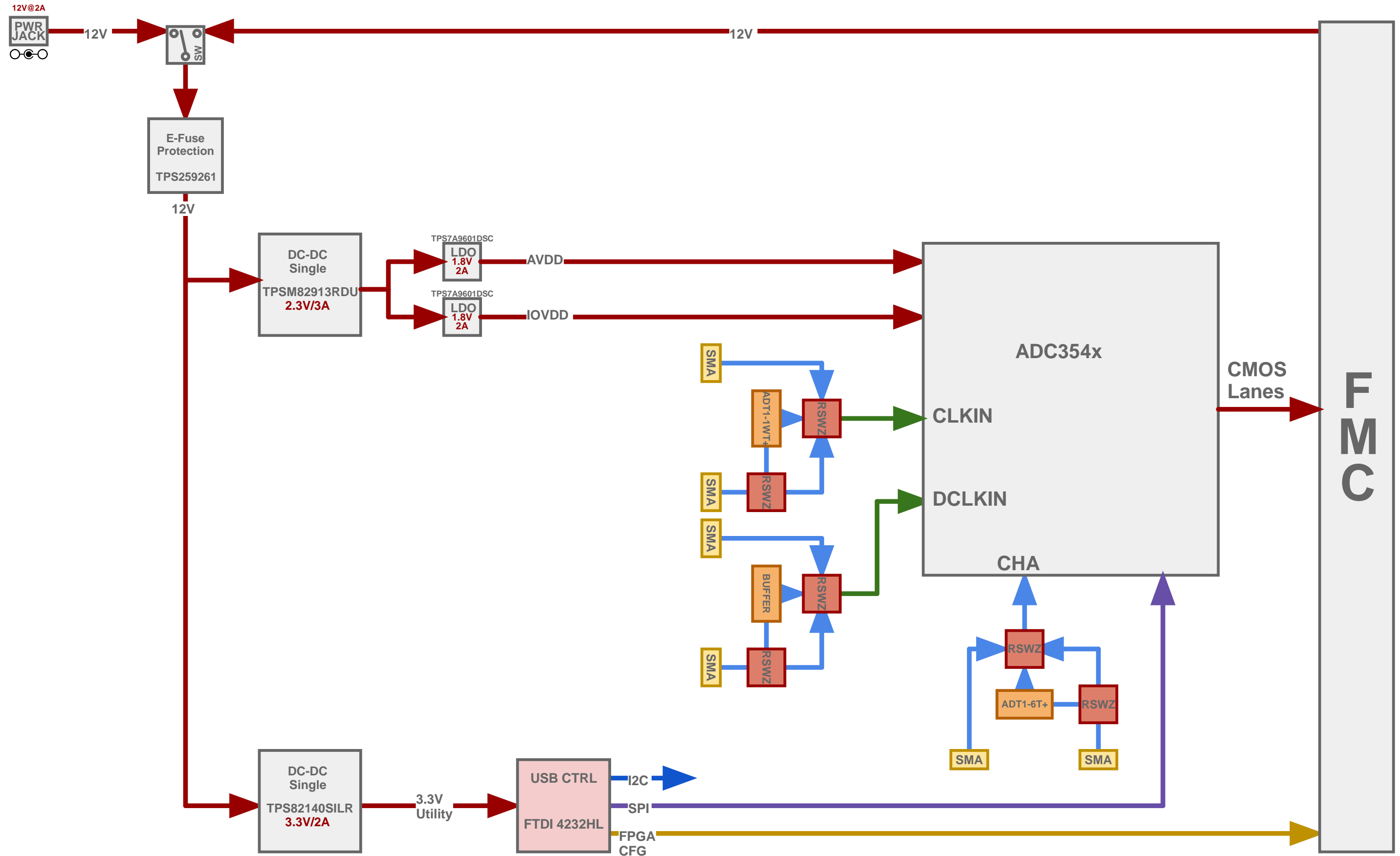

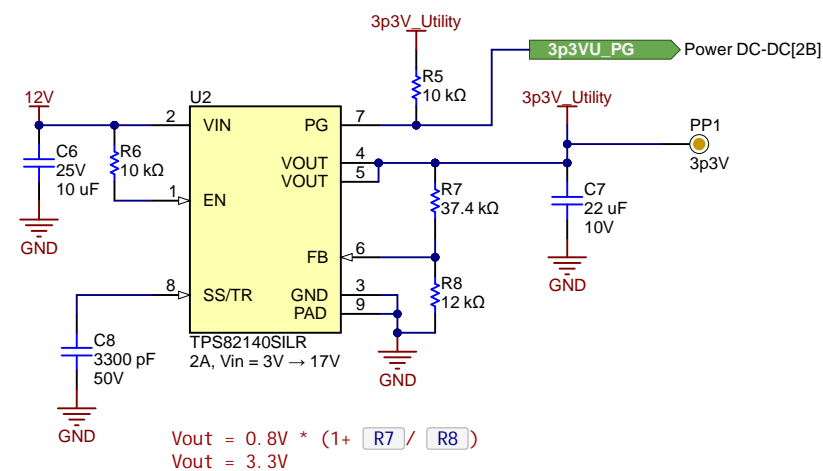
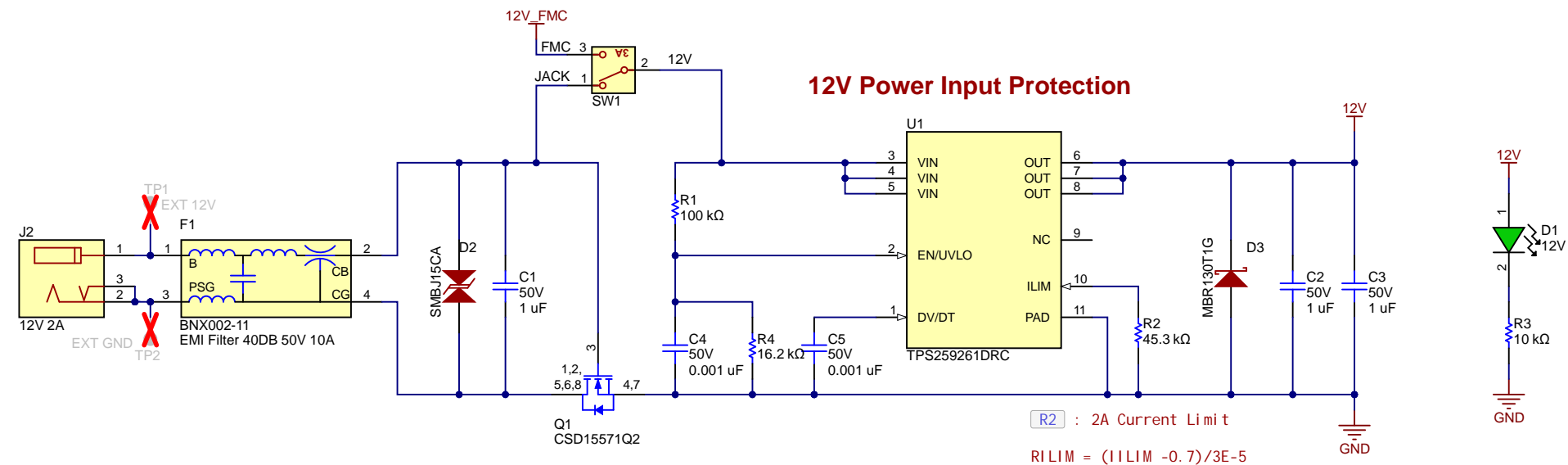



Block Diagram



Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 8/27/2025	 TEXAS INSTRUMENTS http://www.ti.com © Texas Instruments 2025
TID #: N/A	Project Title: ADC3543EVM		
Number: DC092	Rev: G2	Sheet Title: Block Diagram	
SVN Rev: cd68fcb28e835ee311723224187c2400902 (ADC3544)		Sheet: 1 of 15	
Drawn By:		File: Block Diagram.SchDoc	
Engineer: FBR	Contact: http://www.ti.com/support		Size: B

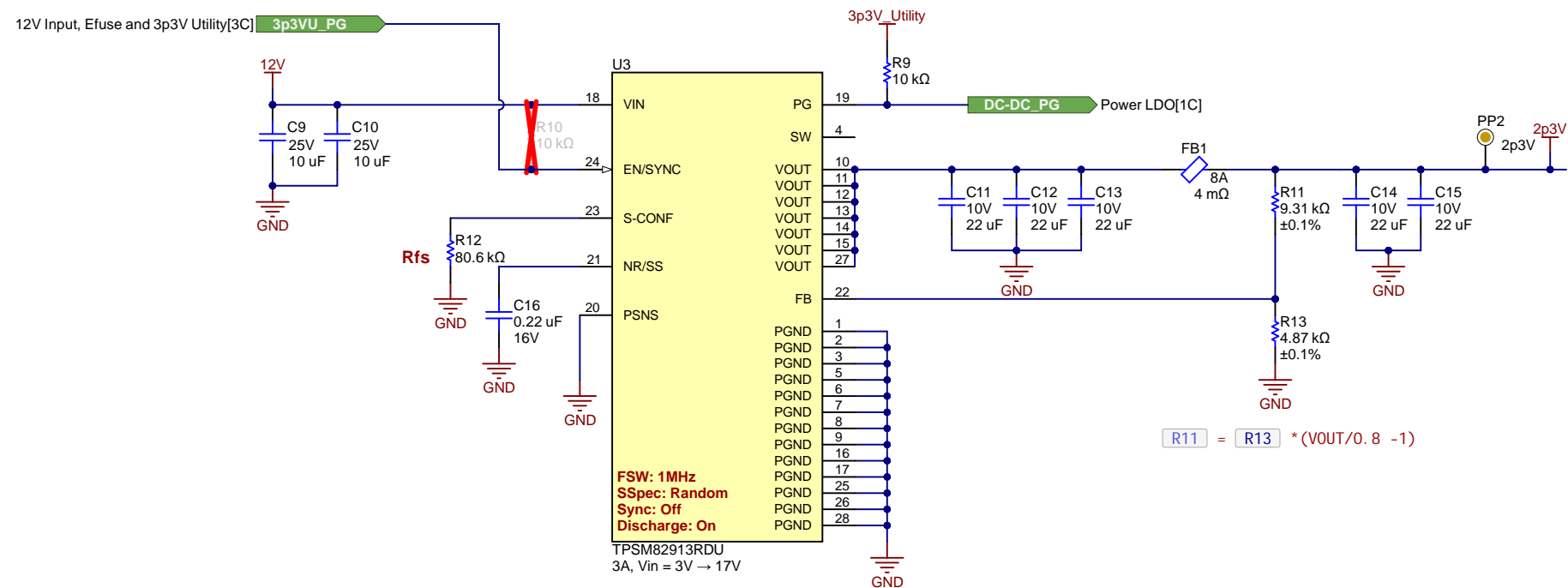
12V Input & 3.3V Utility




Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 8/27/2025	 http://www.ti.com © Texas Instruments 2025
TID #: NA	Project Title: ADC3543EVM		
Number: DC092	Rev: G2	Sheet Title: 12V Input & 3.3V Utility	
SVN Rev: a1d96a7f755630a3c9ea7e5e7d1120034008		Sheet: 2 of 15	
Drawn By:		File: 12V Input, Efuse and 3p3V Utility.SchDoc	
Engineer: FBR		Contact: http://www.ti.com/support	

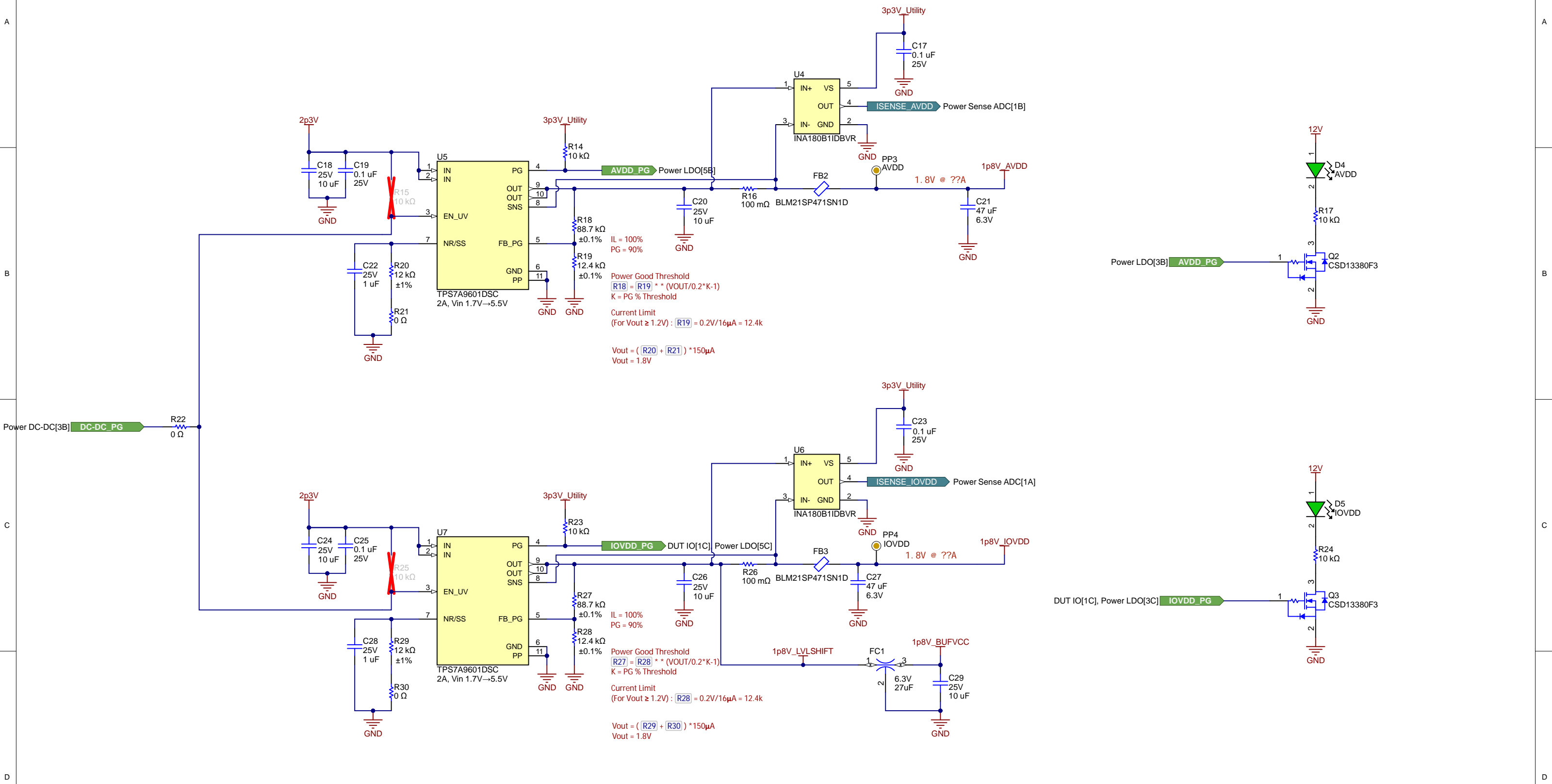
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DC/DC regulator



Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 8/27/2025	
TID #: N/A	Project Title: ADC3543EVM		
Number: DC092	Rev: G2	Sheet Title: DC-DC regulator	
SVN Rev: a1d96a7f755630a3c9ea4a5e7d712003a4008	As of: 12/03/2023	Sheet: 3 of 15	
Drawn By:	File: Power DC-DC.SchDoc	Size: B	
Engineer: FBR	Contact: http://www.ti.com/support		http://www.ti.com © Texas Instruments 2025

LDOs

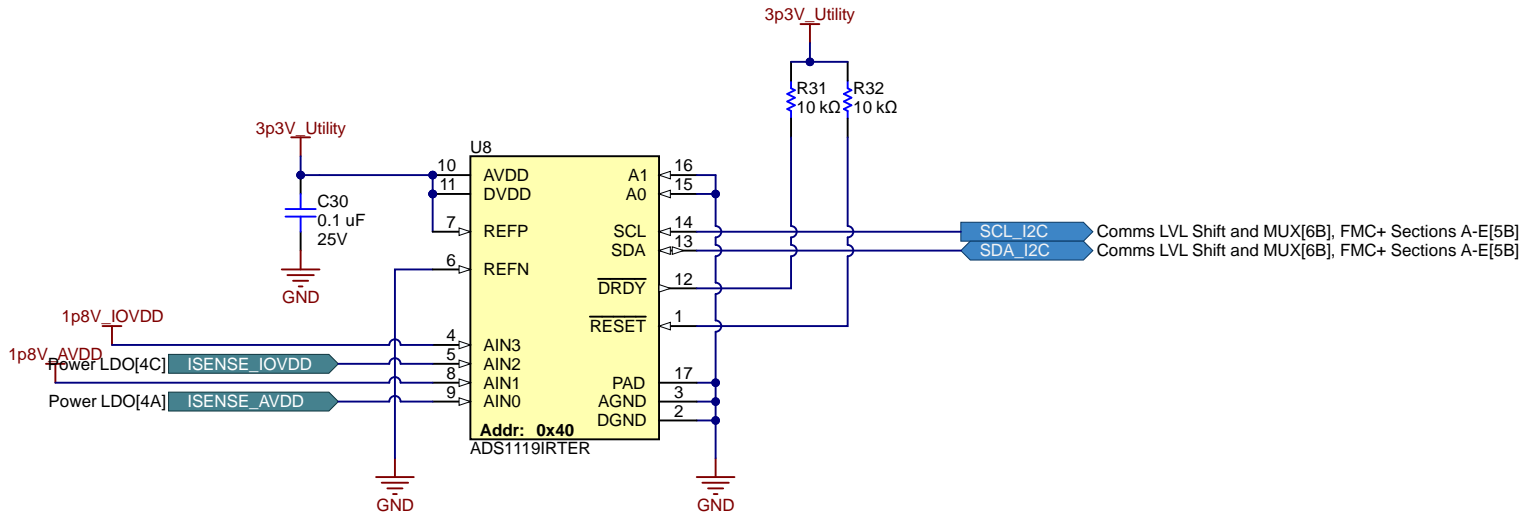


Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 8/27/2025
TID #: N/A	Project Title: ADC3543EVM	
Number: DC092	Rev: G2	Sheet Title: LDOs
SVN Rev: a1d96a7f755630a3c9ea7458712003a4008	Part Number: LDOs (ADC3544)	Sheet: 4 of 15
Drawn By:	File: Power LDO.SchDoc	Size: B
Engineer: FBR	Contact: http://www.ti.com/support	



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Sense ADC



ADS1119RTE Addresses		
A0	A1	Addr
GND	GND	0x40
GND	DVDD	0x41
GND	SDA	0x42
GND	SCL	0x43
DVDD	GND	0x44
DVDD	DVDD	0x45
DVDD	SDA	0x46
DVDD	SCL	0x47
SDA	GND	0x48
SDA	DVDD	0x49
SDA	SDA	0x4A
SDA	SCL	0x4B
SCL	GND	0x4C
SCL	DVDD	0x4D
SCL	SDA	0x4E
SCL	SCL	0x4F

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Orderable: ChangeMe in variant		Designed for: Public Release	Mod. Date: 8/27/2025
TID #: N/A		Project Title: ADC3543EVM	
Number: DC092	Rev: G2	Sheet Title: Sense ADC	
SVN Rev: a1d96a7f755630a3c9ea7a1871200344038		ADC3544	Sheet: 5 of 15
Drawn By: FBR		File: Power Sense ADC.SchDoc	Size: B
Engineer: FBR		Contact: http://www.ti.com/support	

FTDI Control

A

B

C

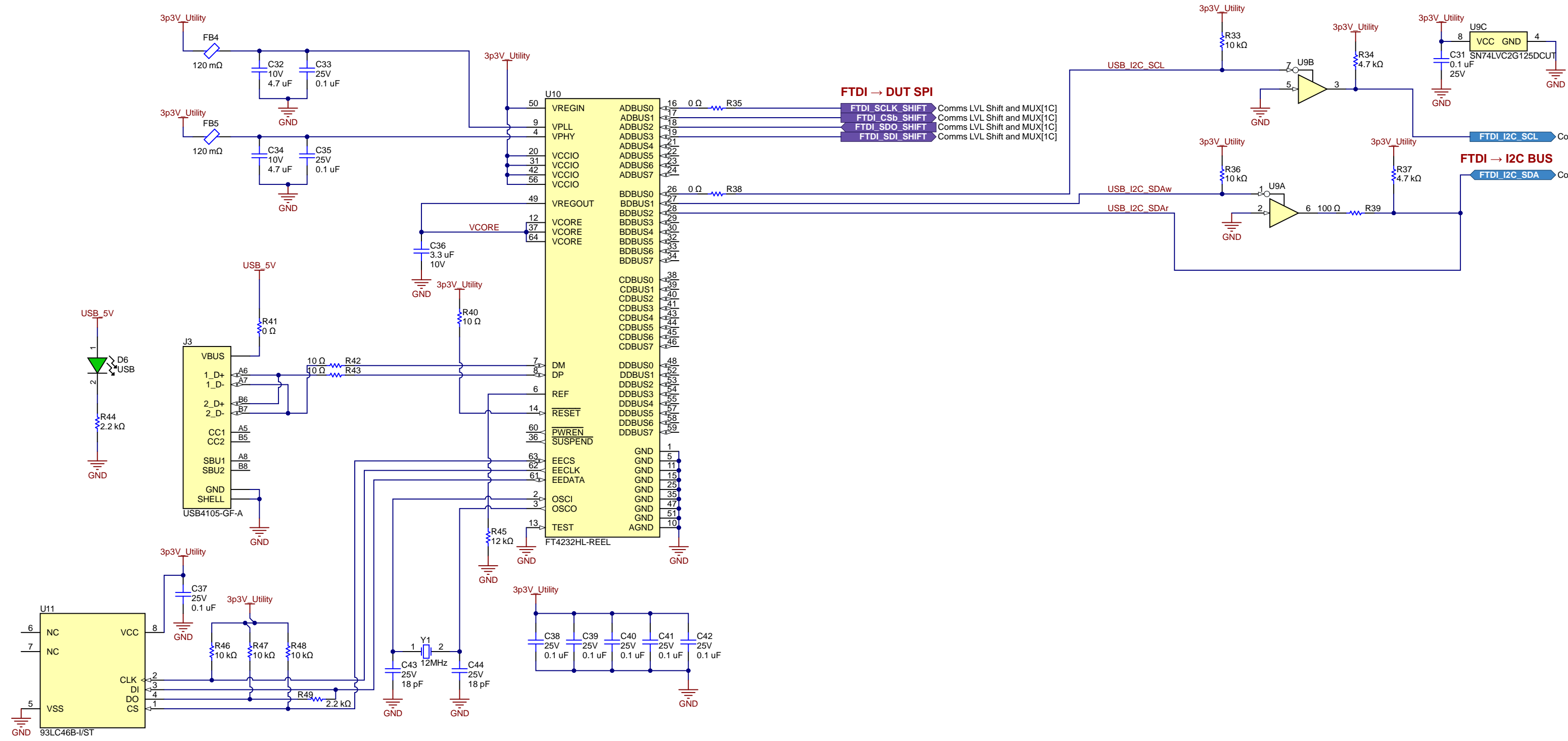
D

A


B

C

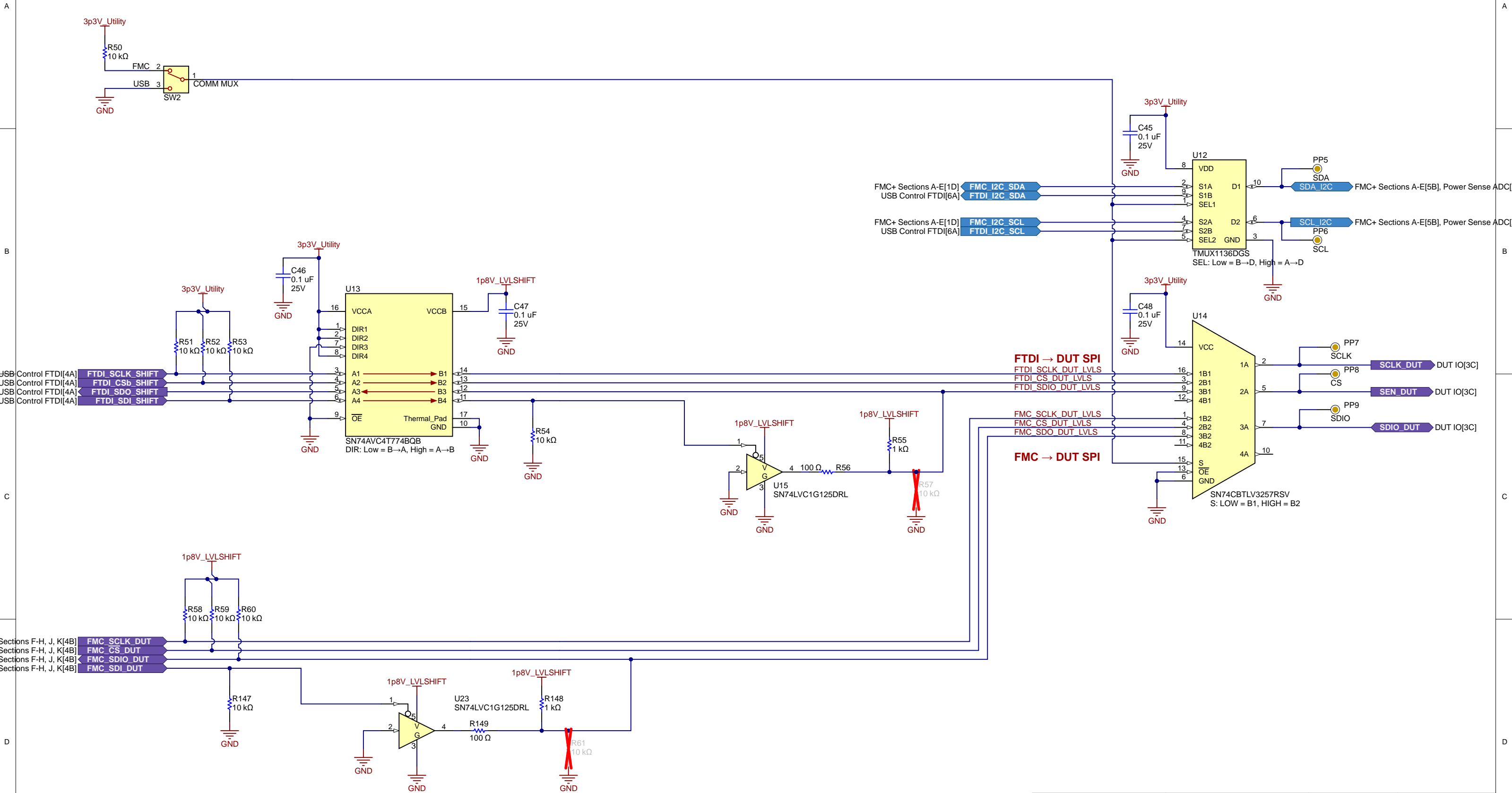
D



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Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 8/27/2025	 TEXAS INSTRUMENTS http://www.ti.com © Texas Instruments 2025
TID #: N/A	Project Title: ADC3543EVM	Sheet Title: FTDI Control	
Number: DC092	Rev: G2	File: USB Control FTDI.SchDoc	
SVN Rev: a1d96a7f755630a3c9ea7a5a711200344003	Sheet: 6 of 15	Size: B	
Drawn By: FBR	Contact: http://www.ti.com/support		

Comms Lvl Shift & Mux



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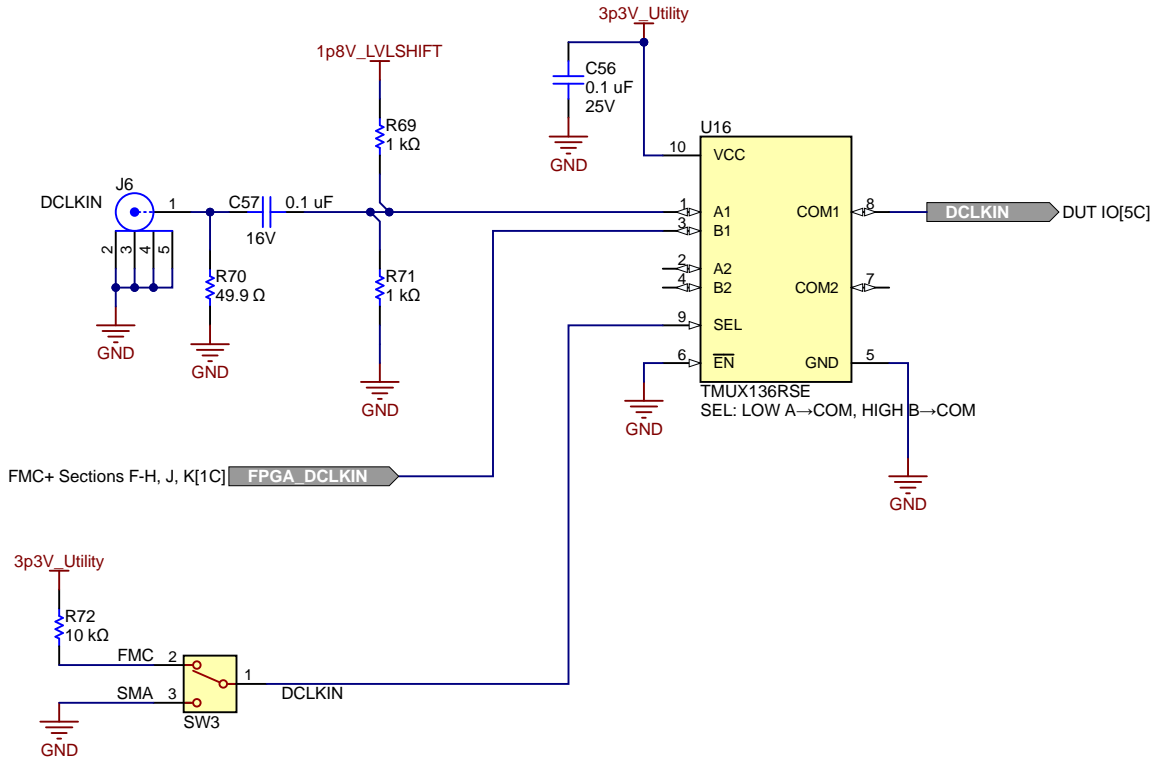
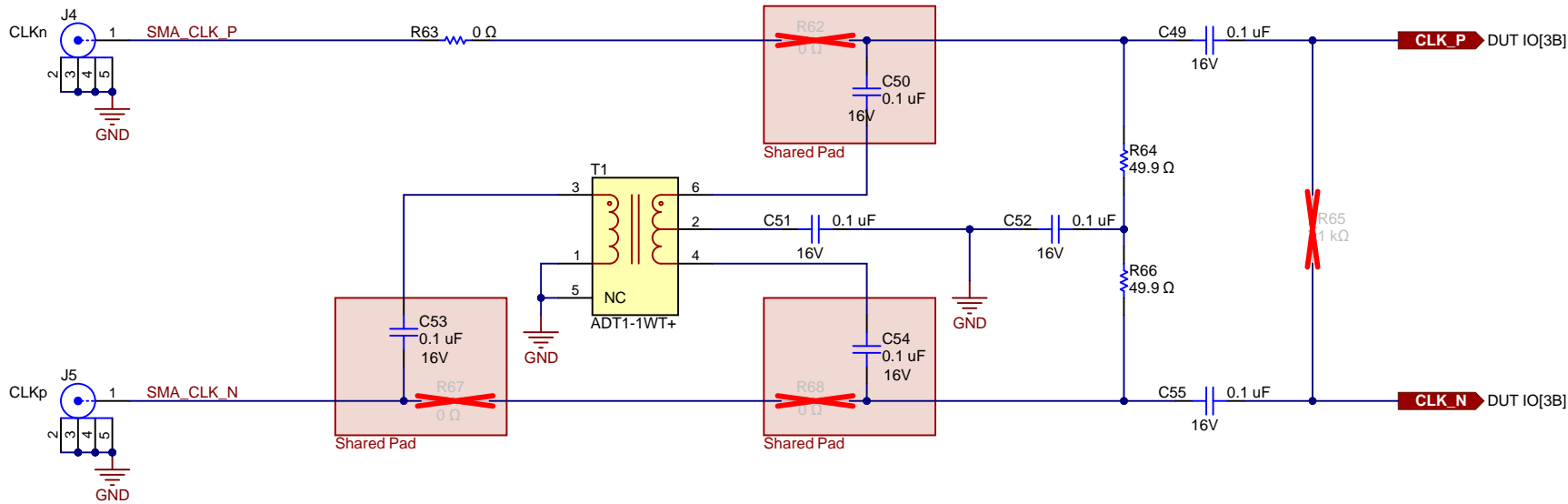
Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 8/27/2025
TID #: N/A	Project Title: ADC3543EVM	
Number: DC092	Rev: G2	Sheet Title: Comms Lvl Shift & Mux
SVN Rev: 42e4b712ead0829c82aa00656b17065615592	File: Comms LVL Shift and MUX.SchDoc	Sheet: 7 of 15
Drawn By: FBR	Contact: http://www.ti.com/support	Size: B
Engineer: FBR		



CLK & DCLKIN

CLK

DCLKIN



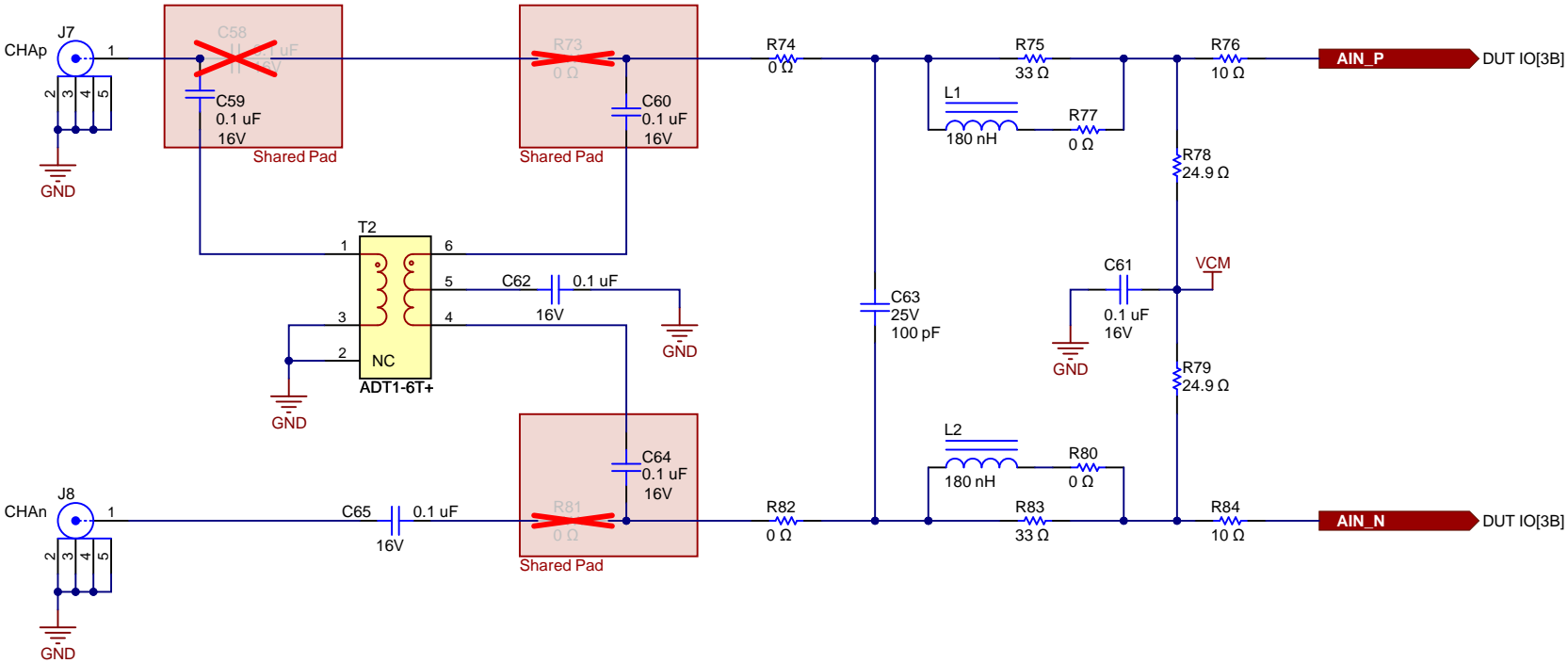
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Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 8/27/2025
TID #: N/A	Project Title: ADC3543EVM	
Number: DC092	Rev: G2	Sheet Title: CLK & DCLKIN
SVN Rev: af9d57260337dc44ad3f657b1e1294068a05802	File: CLK and DCLKIN.SchDoc	Sheet: 8 of 15
Drawn By: FBR	Contact: http://www.ti.com/support	Size: B



ADC Inputs

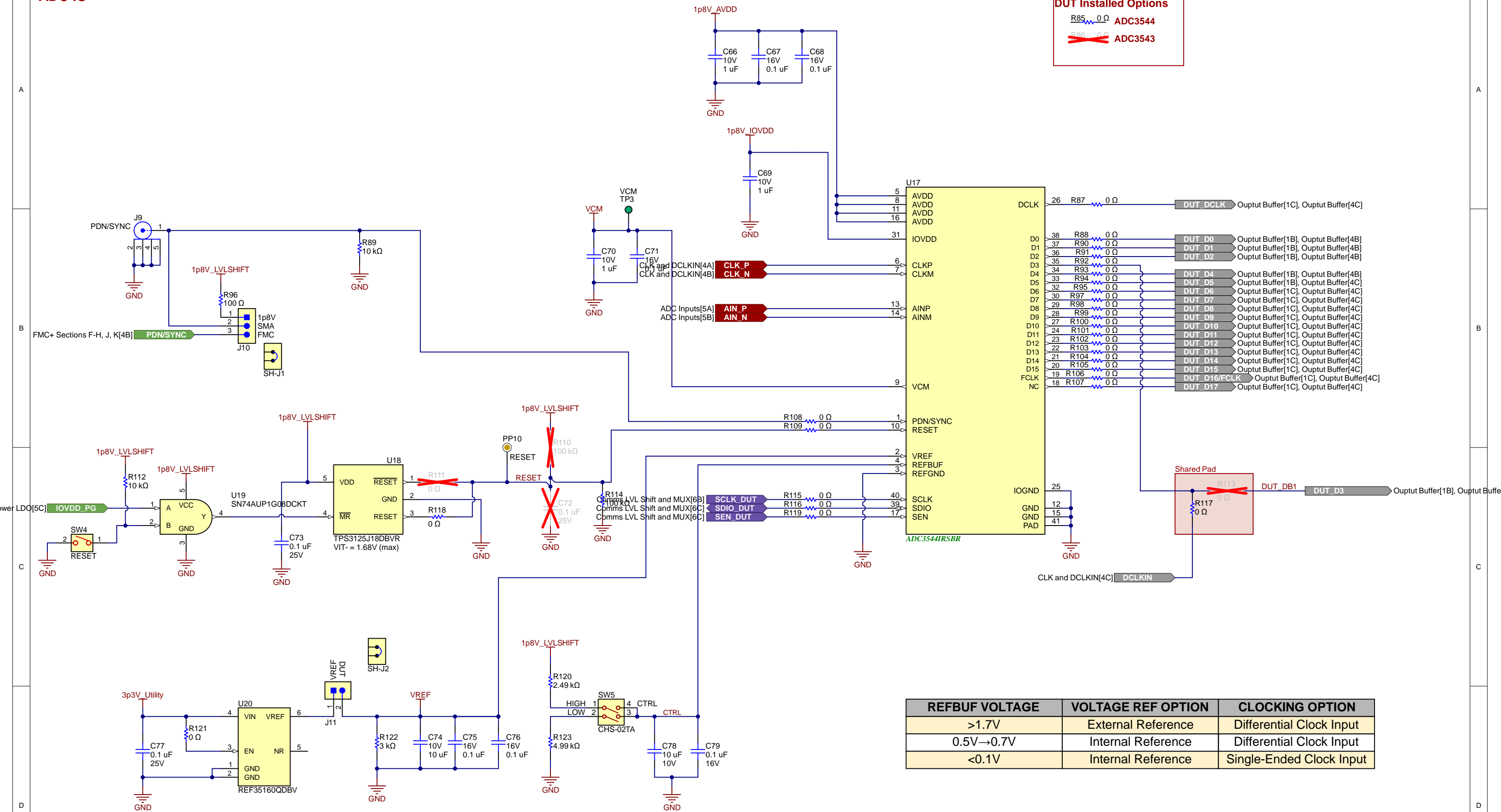
CH A



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Orderable: ChangeMe in variant		Designed for: Public Release	Mod. Date: 8/27/2025
TID #: N/A		Project Title: ADC3543EVM	
Number: DC092	Rev: G2	Sheet Title: ADC Inputs	
SVN Rev: af9d57260337dc44ad3f657b11294062a05802		ADC3544	Sheet: 9 of 15
Drawn By: FBR		File: ADC Inputs.SchDoc	Size: B
Engineer: FBR		Contact: http://www.ti.com/support	

ADC IO



REFBUF VOLTAGE	VOLTAGE REF OPTION	CLOCKING OPTION
>1.7V	External Reference	Differential Clock Input
0.5V→0.7V	Internal Reference	Differential Clock Input
<0.1V	Internal Reference	Single-Ended Clock Input

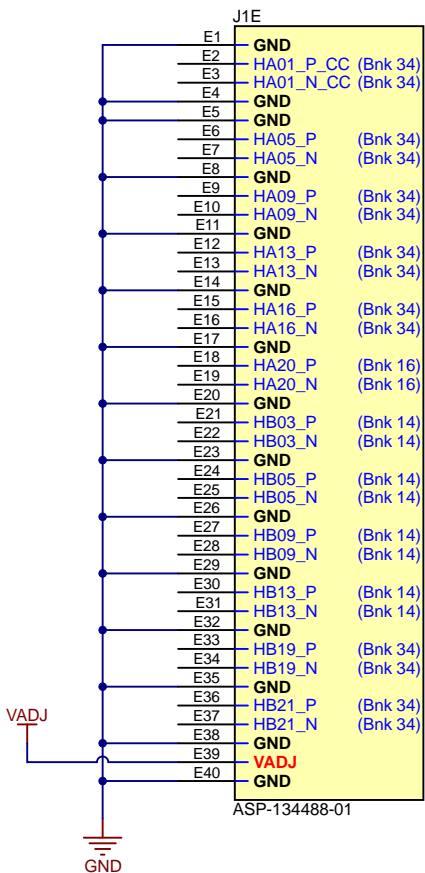
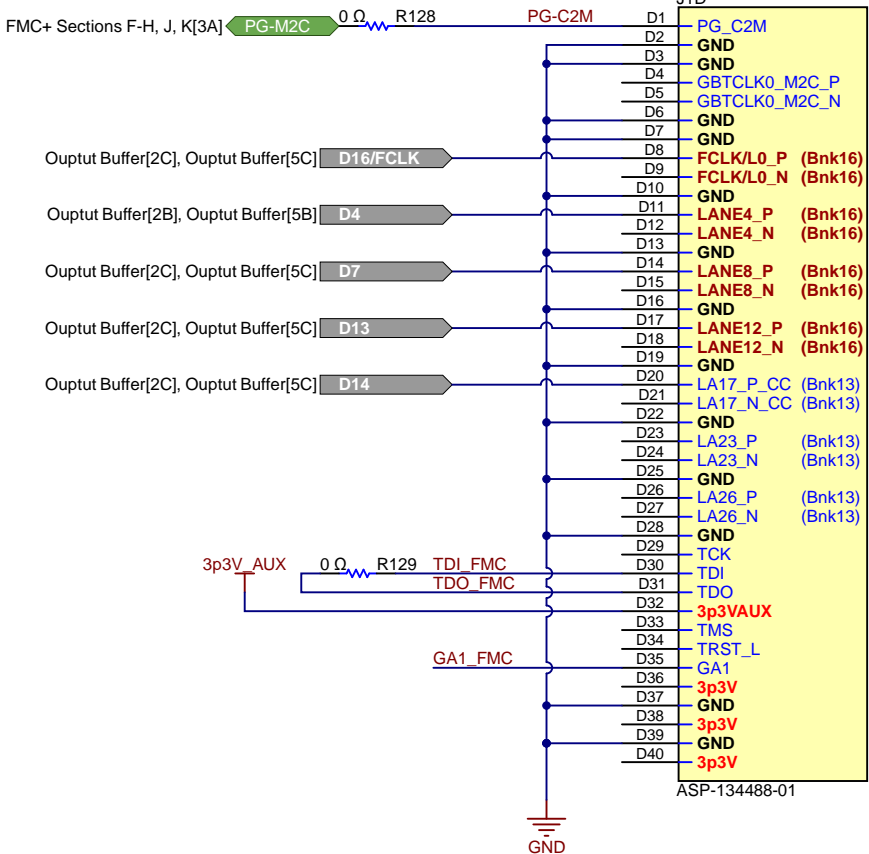
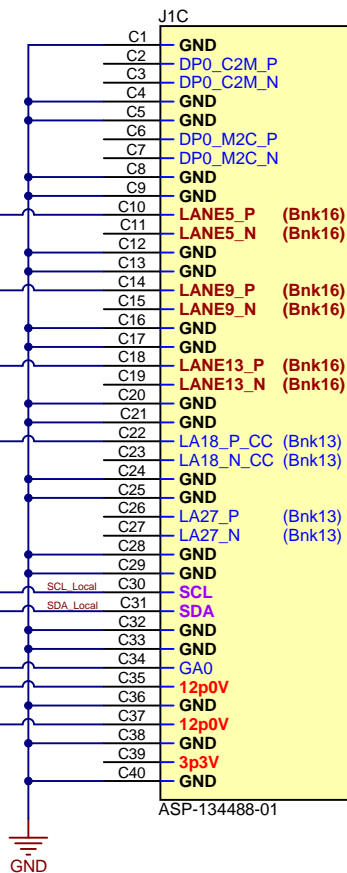
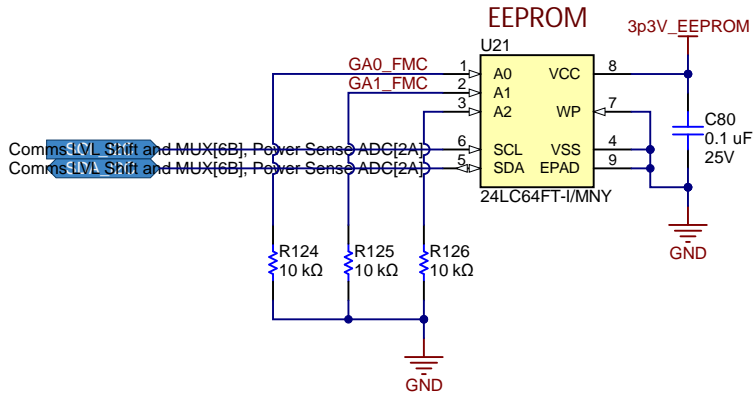
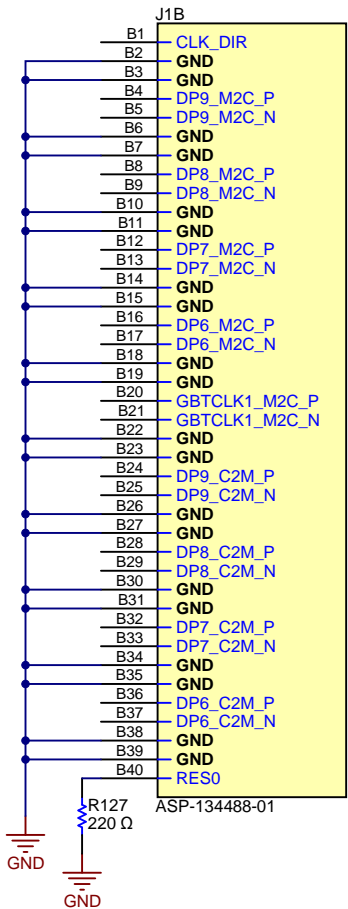
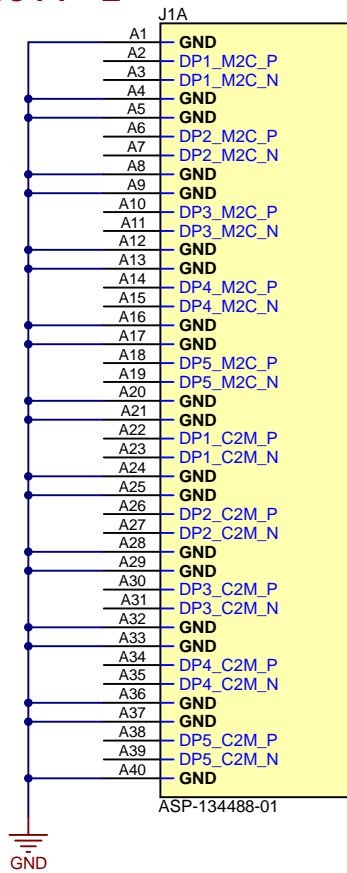
FMC+ Section Rows A - E

A

B

C

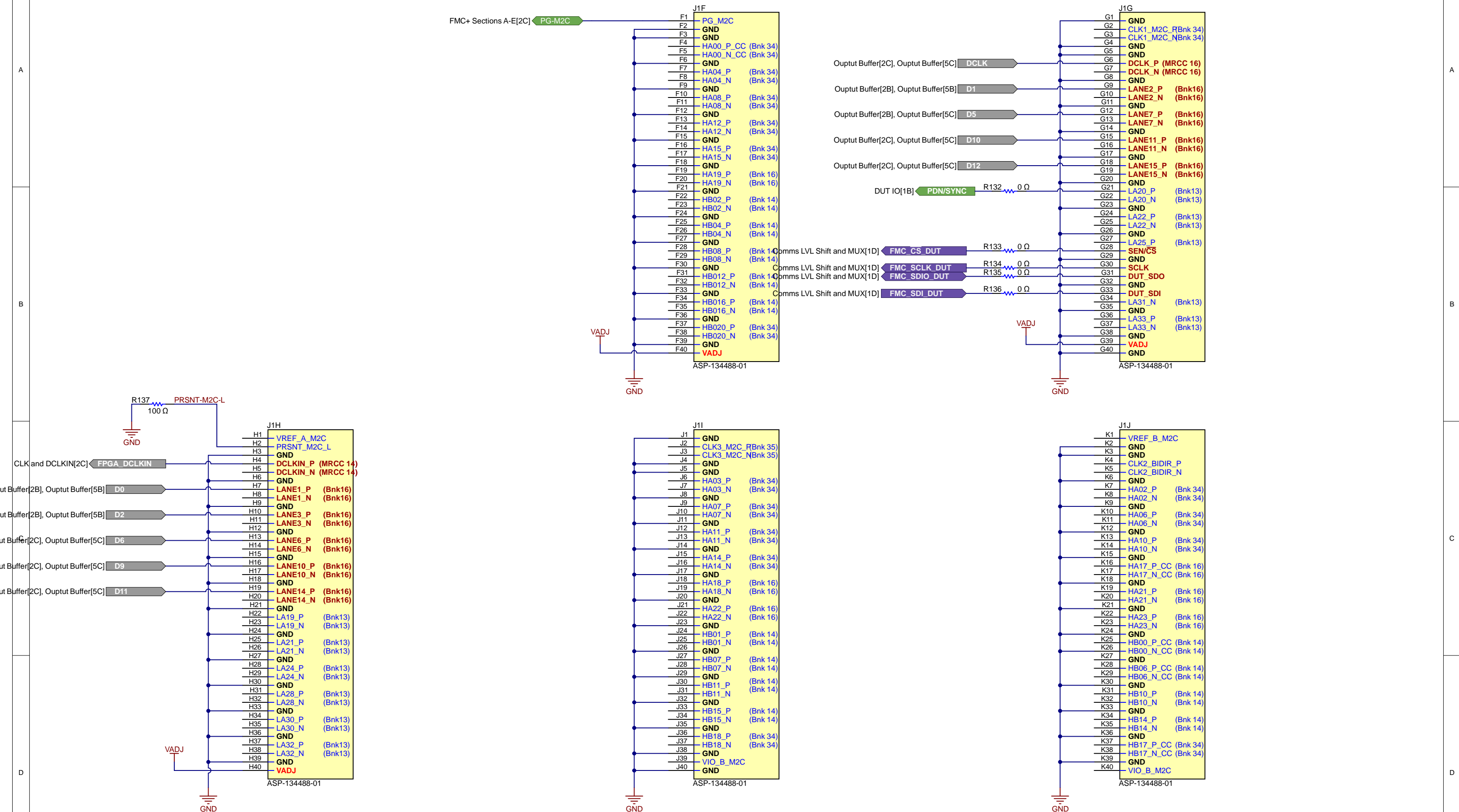
D



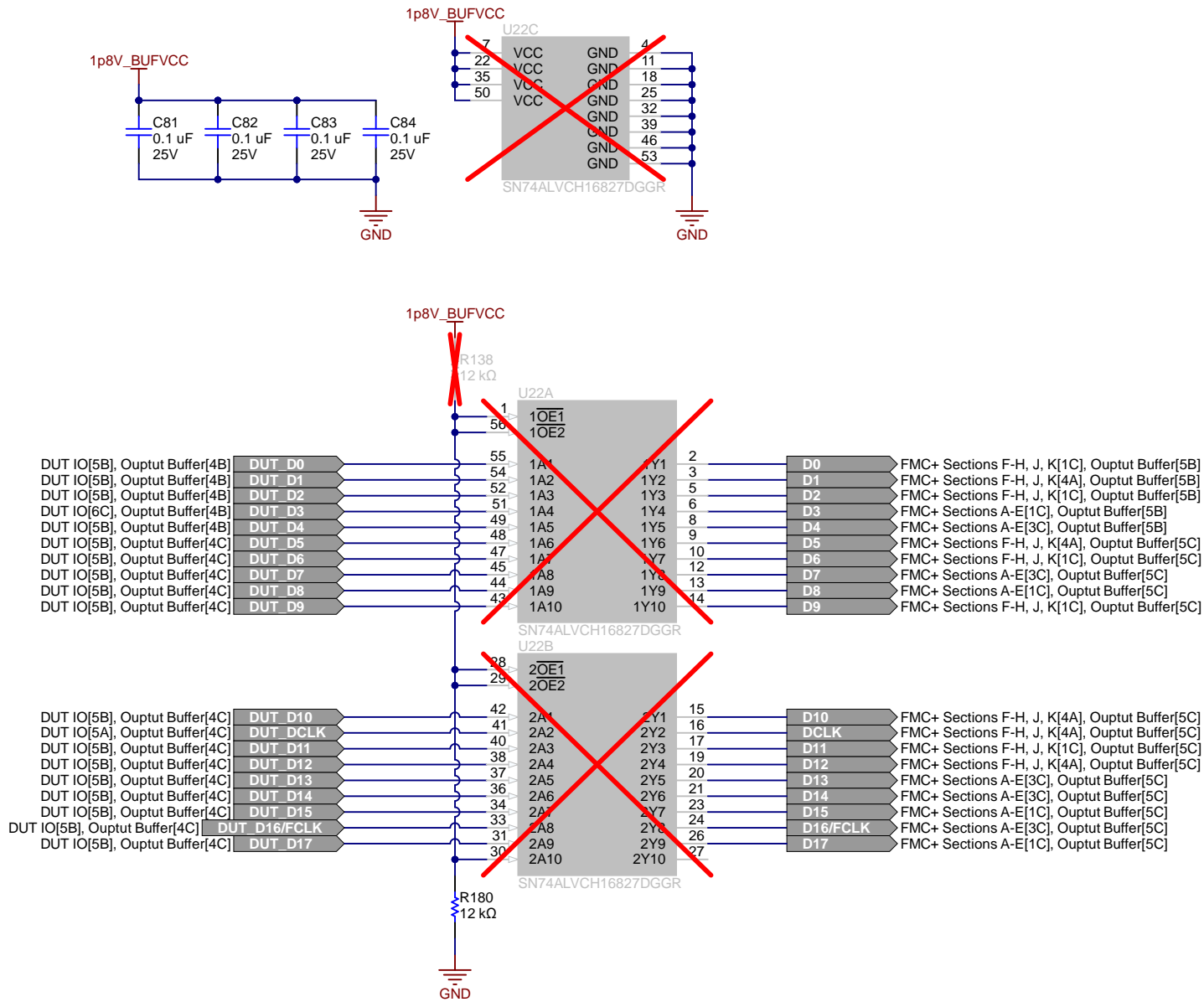
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Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 8/27/2025
TID #: N/A	Project Title: ADC3543EVM	
Number: DC092	Rev: G2	Sheet Title: FMC+ Section Rows A - E
SVN Rev: a1d96a7f755630a3c9ea7a1b71200344038	ADC3544	Sheet: 11 of 15
Drawn By:	File: FMC+ Sections A-E.SchDoc	Size: B
Engineer: FBR	Contact: http://www.ti.com/support	

FMC+ Section Rows F - H, J, K



Output Buffer



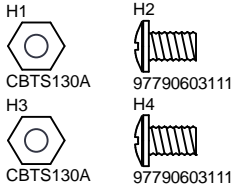
DUT IO[5B], Ouptut Buffer[1B]	DUT_D0	R139	0 Ω	0 Ω	R140	D0	FMC+ Sections F-H, J, K[1C], Ouptut Buffer[2B]
DUT IO[5B], Ouptut Buffer[1B]	DUT_D1	R141	0 Ω	0 Ω	R142	D1	FMC+ Sections F-H, J, K[4A], Ouptut Buffer[2B]
DUT IO[5B], Ouptut Buffer[1B]	DUT_D2	R143	0 Ω	0 Ω	R144	D2	FMC+ Sections F-H, J, K[1C], Ouptut Buffer[2B]
DUT IO[6C], Ouptut Buffer[1B]	DUT_D3	R145	0 Ω	0 Ω	R146	D3	FMC+ Sections A-E[1C], Ouptut Buffer[2B]
DUT IO[5B], Ouptut Buffer[1B]	DUT_D4	R150	0 Ω	0 Ω	R151	D4	FMC+ Sections A-E[3C], Ouptut Buffer[2B]
DUT IO[5B], Ouptut Buffer[1B]	DUT_D5	R152	0 Ω	0 Ω	R153	D5	FMC+ Sections F-H, J, K[4A], Ouptut Buffer[2B]
DUT IO[5B], Ouptut Buffer[1C]	DUT_D6	R154	0 Ω	0 Ω	R155	D6	FMC+ Sections F-H, J, K[1C], Ouptut Buffer[2C]
DUT IO[5B], Ouptut Buffer[1C]	DUT_D7	R156	0 Ω	0 Ω	R157	D7	FMC+ Sections A-E[3C], Ouptut Buffer[2C]
DUT IO[5B], Ouptut Buffer[1C]	DUT_D8	R158	0 Ω	0 Ω	R159	D8	FMC+ Sections A-E[1C], Ouptut Buffer[2C]
DUT IO[5B], Ouptut Buffer[1C]	DUT_D9	R160	0 Ω	0 Ω	R161	D9	FMC+ Sections F-H, J, K[1C], Ouptut Buffer[2C]

DUT IO[5B], Ouptut Buffer[1C]	DUT_D10	R162	0 Ω	0 Ω	R163	D10	FMC+ Sections F-H, J, K[4A], Ouptut Buffer[2C]
DUT IO[5A], Ouptut Buffer[1C]	DUT_DCLK	R164	0 Ω	0 Ω	R165	DCLK	FMC+ Sections F-H, J, K[4A], Ouptut Buffer[2C]
DUT IO[5B], Ouptut Buffer[1C]	DUT_D11	R166	0 Ω	0 Ω	R167	D11	FMC+ Sections F-H, J, K[1C], Ouptut Buffer[2C]
DUT IO[5B], Ouptut Buffer[1C]	DUT_D12	R168	0 Ω	0 Ω	R169	D12	FMC+ Sections F-H, J, K[4A], Ouptut Buffer[2C]
DUT IO[5B], Ouptut Buffer[1C]	DUT_D13	R170	0 Ω	0 Ω	R171	D13	FMC+ Sections A-E[3C], Ouptut Buffer[2C]
DUT IO[5B], Ouptut Buffer[1C]	DUT_D14	R172	0 Ω	0 Ω	R173	D14	FMC+ Sections A-E[3C], Ouptut Buffer[2C]
DUT IO[5B], Ouptut Buffer[1C]	DUT_D15	R174	0 Ω	0 Ω	R175	D15	FMC+ Sections A-E[1C], Ouptut Buffer[2C]
DUT IO[5B], Ouptut Buffer[1C]	DUT_D16/FCLK	R176	0 Ω	0 Ω	R177	D16/FCLK	FMC+ Sections A-E[3C], Ouptut Buffer[2C]
DUT IO[5B], Ouptut Buffer[1C]	DUT_D17	R178	0 Ω	0 Ω	R179	D17	FMC+ Sections A-E[1C], Ouptut Buffer[2C]

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Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 8/27/2025
TID #: N/A	Project Title: ADC3543EVM	
Number: DC092	Rev: G2	Sheet Title: Output Buffer
SVN Rev: a1d96a7f755630a3c9ea76187d11200344038	File: Ouptut Buffer.SchDoc	Size: B
Drawn By: FBR	Contact: http://www.ti.com/support	

Hardware & Mechanicals



PCB Number: DC092

PCB Rev: G2



PCB

LOGO

FCC disclaimer



LBL1

PCB Label

THT-14-423-10

Size: 0.65"x0.20"

ZZ1

Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

-

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Orderable: ChangeMe in variant		Designed for: Public Release	Mod. Date: 8/27/2025
TID #: N/A		Project Title: ADC3543EVM	
Number: DC092	Rev: G2	Sheet Title: Hardware & Mechanicals	
SVN Rev: a1d96a7f755630a3c9ea7d8a7d1200344038		Assembled by: 1200344038	Sheet: 14 of 15
Drawn By:		File: Hardware & Mechanicals.SchDoc	Size: B
Engineer: FBR		Contact: http://www.ti.com/support	

Rev History & Variants

Revision History

Rev	Release Date	Notes
G	Feb - 2024	Complete redesign of EVM

Variant(s)

Variant	Notes
001 (ADC3543)	U1: ADC3543 DNI: TP1, TP2, R10, R15, R23, R55, R59, R60, R63, R65, R66, R67, R68, C63, R83, R91, C71, R95, R103, R112, R76, (BUFFER BYPASS), R107, R109
002 (ADC3544)	U1: ADC3544 DNI: TP1, TP2, R10, R15, R23, R55, R59, R60, R63, R65, R66, R67, R68, C63, R83, R91, C71, R95, R103, R112, R76, (BUFFER BYPASS), R107, R109

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Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 8/27/2025
TID #: N/A	Project Title: ADC3543EVM	
Number: DC092	Rev: G2	Sheet Title: Rev History & Variants
SVN Rev: cc12e20264b0e2993bad78a9159c363b8608	Base Part: ADC3543	Sheet: 15 of 15
Drawn By: FBR	File: Revision History.SchDoc	Size: B
Engineer: FBR	Contact: http://www.ti.com/support	